UNITED STATES PATENT APPLICATION

for

SPREAD SPECTRUM CLOCKING TOLERANT RECEIVERS

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SPREAD SPECTRUM CLOCKING TOLERANT RECEIVERS

BACKGROUND OF THE INVENTION

TECHNICAL FIELD OF THE INVENTION

The present invention relates to semiconductor transmitting and receiving chips and, more particularly, to receivers in the receiving chips that are spread spectrum clocking tolerant.

BACKGROUND ART:

Spread spectrum clocking (SSC) has become ubiquitous in the personal computer industry for controlling electromagnetic emissions. FIG. 1 illustrates a typical SSC scheme in which the frequency of a clock signal changes in a triangular waveform between a maximum frequency (fmax) and a minimum frequency (fmin) that is equal to 0.995 fmax. The frequency of triangular waveform is typically about 30kHz. However, fmax is many times greater (e.g., 100MHz or higher).

In desktop personal computers, where common clock architectures dominate, the impact of SSC is minimal and, currently, no design changes are generally required to reap electromagnetic interference (EMI) benefit from SSC, which may be any where up to around 20dB. Accordingly, almost all personal computer systems shipped today have SSC implemented.

In some computer systems and communications devices and systems, a clock is embedded in the data for input/output (I/O) or other signals. An example of a data signal with an embedded clock is one using the 8b/10b (8-bit/10-bit) coding scheme. A receiver including a receiving gate that gates the data signal to produce a gated data signal. The receiver also include clock recovery circuitry to extract clock information to create a signal to clock the receiving gate. To date, SSC proliferation in embedded clock systems has been limited due to the inability of present receivers to track the kHz modulation frequency variations. That is, the receivers have difficulty differentiating between deliberate frequency changes and unintentional jitter on the clock. An example of such a receiver is an interpolator based receiver. In some

interpolator based receivers, a local reference clock is used in conjunction with the embedded clock information to determine the optimum timing for gating data.

For example, FIG. 2 illustrates a prior art system 10 in which a transmitting chip 14 transmits a data signal with embedded clock information to a receiving chip 16 over an interconnect 18. The clock information may be embedded through a coding technique such as 8b/10b or some other technique. Transmitter 22, in transmitting chip 14, transmits the data signal in response to a transmitting clock signal that has a constant frequency rather than SSC. Transmitter 22, interconnect 18, and an interpolator based receiver 24 in receiving chip 16 may form a point to point serial link. Receiver 24 includes a receiving gate 26 and clock recovery circuitry 28. In the example of FIG. 2, the clock recovery circuitry 28 includes a phase detector 32 (for example, an edge detector) and a phase interpolator 30. Receiving gate 26 receives the data signal on interconnect 18 and a clock signal from phase interpolator 30 referred to herein as the "in phase clock signal" because it is in phase with the data signal on interconnect 18. The in phase clock signal gates receiving gate 26 to produce the gated data signal from the data signal on interconnect 18.

Phase detector 32 analyzes the data signal on interconnect 18 to extract phase information regarding the data signal. The phase information is included in a phase information signal provided to phase interpolator 30. A local reference source 34 provides a reference clock signal which has a frequency which is very close (and ideally identical) to the frequency of the transmitting clock signal provided to transmitter 22. Phase interpolator 30 creates the in phase clock signal through using the reference clock signal from local reference source 34 and the phase information signal from phase detector 32.

As noted, the transmitting clock signal applied to transmitter 22 has a constant frequency. (Of course, there is some unintended jitter in the clock.) If instead, a SSC clock, were applied to transmitter 22, interpolator 30 would not, in many cases, be able to differentiate between the deliberate frequency movement of SSC and the unintentional jitter on the clock. Accordingly, the in phase clock signal would not always actually be in phase and some of the data signal would not be gated at a correct time.

There are various ways in which to implement an interpolator based receiver such as the one shown in system 10 of FIG. 2. It takes time for phase detector 32 and phase interpolator 30 to perform their functions. Under one approach, there is a delay in receiving gate 26 so that the portion of the data signal that is being gated is gated by an in phase clock signal generated through phase interpolator 30 and phase detector 32 in response to the same portion of the data signal. Under another approach, there is no delay or just a slight delay so that a portion of the data signal is gated in response to a portion of the in phase clock signal generated in response to a previous portion of the data signal. This is not a problem since the phase of the data signal rarely would change much over such a short amount of time. The phase detector 32 might merely sample some portions of the data signal. Other control circuitry can be used in connection with, for example, test patterns to obtain or retain the in phase clock signal. In some implementations, the edge detector receives data from the output of receiving gate 26 rather than at the input.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

FIG. 1 illustrates a time versus frequency graph of a clock using a commonly used spread spectrum clocking.

FIG. 2 is a schematic representation of a prior art system having a transmitting and receiving chip wherein the receiving chip includes an interpolator based receiver.

FIG. 3 is a schematic representation of a system having a transmitting and receiving chip wherein the receiving chip includes an SSC tolerant interpolator based receiver according to some embodiments of the invention.

FIG. 4 is a schematic representation of a details of a demodulator and RF mixer shown in FIG. 3 according to some embodiments of the invention.

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FIG. 5 is a schematic representation of a details of a demodulator and RF mixer shown in FIG. 3 according to some embodiments of the invention.

FIG. 6 is a schematic representation of a system having a transmitting and receiving chip wherein the receiving chip includes an SSC tolerant interpolator based receiver according to some embodiments of the invention and is an alternative to the implementations of FIG. 3.

FIG. 7 is a schematic representation of a system having a transmitting and receiving chip wherein the receiving chip includes an SSC tolerant interpolator based receiver according to some embodiments of the invention and is an alternative to the implementations of FIG. 3.

DETAILED DESCRIPTION

The invention involves SSC tolerant clock recovery circuitry that provides to a receiving gate, an in phase clock signal that is in phase with a data signal and mirrors frequency changes in the data signal and with the SSC transmitting clock which causes the SSC changes in frequency. In this way, the invention solves the limitations of the prior art system. FIGS. 3-6 illustrate some embodiments of the invention. However, it should be stressed that the invention is not limited to these details. The SSC tolerant nature of the receiver can be implemented with other circuits.

FIG. 3 illustrates a system 50 in which a transmitting chip 54 transmits a data signal with embedded clock information to a receiving chip 56 over an interconnect 58. The clock information may be embedded through a coding technique such as 8b/10b or some other technique. Transmitter 62, in transmitting chip 54, transmits the data signal in response to an SSC transmitting clock signal. SSC transmitting clock signal may have the characteristics of the signal in prior art FIG. 1 or be somewhat different. For example, the difference in fmax and fmin could be greater or less and the frequency of change could be greater or less than is shown in FIG. 1. The data signal may have a phase change or other change that tracks the frequency change in the SSC transmitting clock signal. Transmitter 62, interconnect 58, and a receiver 64 in receiving chip 56 may form a point to point serial link, but the invention is not restricted to point to point. Interconnect 58 may be unidirectional or bi-directional. Interconnect 58 may be differential or single ended.

Receiver 64 includes a receiving gate 66 and a clock recovery circuitry 68. In the embodiment of FIG. 3, clock recovery circuitry 68 includes a phase detector 72, a phase interpolator 70, and mirroring circuitry 80 to create a frequency mirrored clock signal. In the example of FIG. 3, receiver 64 is an interpolator based receiver. Phase detector 72 analyzes the data signal on interconnect 58 to extract phase information regarding the data signal. Phase detector 72 may use edge detection (such as cell edge detection) or some other means of phase detection. The phase information is included in a phase information signal provided to phase interpolator 70. A local reference source 74 produces a reference clock signal which has a frequency which is very close (and ideally identical) to, for example, the maximum or minimum frequency of the SSC transmitting clock signal provided to transmitter 62. However, the reference clock signal has a constant frequency (although it will have some jitter). Local reference source 74 may be internal or external to receiving chip 56.

Phase interpolator 70 creates the in phase clock signal through using the frequency mirrored clock signal and the phase information signal. Receiving gate 66 receives the data signal on interconnect 58 and the in phase clock signal from phase interpolator 70. Because the frequency mirrored clock signal mirrors frequency changes in the data signal, the in phase clock signal will be in phase with the data signal and will gate receiving gate 66 at correct times. The in phase clock signal gates receiving gate 66 to produce the gated data signal from the data signal on interconnect 58.

Mirroring circuitry 80 produces the frequency mirrored clock signal that is provided to phase interpolator 70. There are various ways in which mirroring circuitry 80 can be implemented. One way is through demodulating and RF mixer circuitry, examples of which are illustrated in FIGS. 4 and 5, but the invention is not restricted thereto. Referring to FIG. 4, in some embodiments, mirroring circuitry 80 is demodulator and RF mixer circuitry which includes a low pass filter 88 which extracts the low frequency change in frequencies between fmax and fmin. In the case of FIG. 1, there is a 30kHz change in frequency between fmax and fmin. (Note that the SSC transmitting clock signal does not have to be a triangular shaped wave.) If the SSC transmitting clock signal of FIG. 3 were the clock of FIG. 1, then the output of low pass filter 88 would be primarily or exclusively components of a 30kHz signal. Because

of the coding (e.g., 8b/10b coding), the output of low pass filter 88 may be points rather than continuous wave.

Time interpolator 90 creates a continuous or relatively continuous wave (which may look like that of FIG. 1.) Changes in frequency in the data signal may be translated into changes in amplitude in the output of time interpolator 90. Time interpolator 90 may include histogram analysis to improve efficiency and/or handle changes in direction around fmax and/or fmin. Referring to FIG. 5, time interpolator 98 is shown including the histogram analysis which uses information regarding previously detected waveforms to help more quickly find the correct current waveform. Biasing & amplitude adjusting circuitry 92 makes sure the continuous or relatively continuous wave output of time interpolator 90 or 98 has a proper bias and amplitude to be suitable for an RF mixer 96. RF mixer 96 frequency modulates the output of biasing and amplitude adjusting circuitry 92 with the reference clock signal to produce the frequency mirrored clock signal provided to phase interpolator 70. RF mixer 96 might be called an FM block (frequency modulator block) because RF mixer 96 does frequency modulation. However, the frequencies do not have to be in the radio or FM frequency ranges. As noted, the details of circuitry to create a frequency mirrored clock signal can be somewhat different than those shown in FIGS. 4 and 5.

There are various ways in which to implement an interpolator based receiver such as the one shown in FIG. 3. It takes time for phase detector 72, phase interpolator 70, and mirroring circuitry 80 to perform their functions. Under one approach, there is a delay in receiving gate 66 so that the portion of the data signal that is being gated is gated by an in phase clock signal generated through phase interpolator 70, phase detector 72, and mirroring circuitry 80 in response to the same portion of the data signal. Under another approach, there is no delay or just a slight delay so that a portion of the data signal is gated in response to a portion of the in phase clock signal generated in response to a previous portion of the data signal. This is not a problem since the phase of the data signal rarely would change much over such a short amount of time. The phase detector 72 might merely sample some portions of the data signal. Other control circuitry can be used in connection with, for example, test patterns to obtain or retain the in phase clock signal.

In some implementations, the phase detector receives data from the output of receiving gate 66 rather than at the input. An example of this is provided in FIG. 6, which includes a system 100 which is similar to system 50 except as follows. In system 100, receiving chip 106 includes a receiver 104 with clock recovery circuitry 108. Clock recovery circuitry 108 includes phase detector 112, mirroring circuitry 120, and phase interpolator 70. In FIG. 6, phase detector 112 and mirroring circuitry 120 receive the gated data rather than the data signal as in FIG. 3. Phase detector 112 and mirroring circuitry 120 may be the same as or similar to phase detector 72 and mirroring circuitry 80 in FIG. 3 except that phase detector 112 and mirroring circuitry 120 may be modified to better handle the gated data signal. Training or test data may be passed through interconnect 58 to get a proper phase information signal and frequency mirrored clock signal prior to passing actual data in a data signal on interconnect 58.

Except for the new features and components, the components and features of system 50 illustrated in FIG. 3 can be the same as or similar to those of prior art system 10 in FIG. 2, or some or more of the components and features of system 50 can be somewhat different. For example, receiving gate 66 can be the same as or different than prior art receiving gate 26; phase interpolator 70 can be the same as or different that prior art interpolator 30, etc.

The SSC transmitting clock signal may be a continuous signal or only operate at around the time data is to be transmitted. Likewise, local reference source 74 may provide the reference clock signal continuously or only around the time data is to be transmitted.

FIG. 7 illustrates an alternative embodiment without the use of a reference clock. Referring to FIG. 7, system 150 is similar to system 50 except that receiving chip 156 includes receiver 154 which in turn includes receiving gate 66 and a clock recovery circuitry 158. Clock recovery circuitry 158 includes a phase detector 72 and SSC frequency information circuitry 160 which produces a frequency mirrored clock signal that mirrors frequency changes in the data signal for phase interpolator 70. SSC frequency information circuitry 160 uses training information, and perhaps a demodulator like that of FIG. 4 or 5, to determine the frequency changing pattern of the data signal as well as the actual frequencies to produce the frequency mirrored clock signal. Following the training data, the frequency change information can be kept updated with additional readings of the data signal. There could be an implementation of

system 150 like that of FIG. 6 where the phase detector and/or SSC frequency information circuitry receive inputs from the output of receiving gate 66.

There may be additional circuitry in the chips that is not illustrated such as electrostatic discharge circuitry on interconnect 58.

It is noted that in this disclosures, when it is said one signal is in phase with another it means it is very close to being exactly in phase. When it is said one signal mirrors frequency changes in another it means it is very close to exactly mirroring frequency changes. There will always be some error. Through engineering choices the desired closeness can be increased. The functional matter is whether the gating is done within acceptable tolerances so the proper data is gated from the data signal.

Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments, of the invention. The various appearances "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments.

If the specification states a component, feature, structure, or characteristic "may", "might", or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the element. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

Those skilled in the art having the benefit of this disclosure will appreciate that many other variations from the foregoing description and drawings may be made within the scope of the present invention. Accordingly, it is the following claims including any amendments thereto that define the scope of the invention.